Preliminary Amendment
Applicant: Michael Goessel et al.
Serial No.: Unknown
(Priority Application No. DE 103 49 933.4)
(International Application No. PCT/US2004/002362)
Filed: Herewith
(Priority Date: October 24, 2003)
(International Filing Date: October 22, 2004)
Docket No.: I431.135.101
Title: EVALUATION CIRCUIT AND METHOD FOR DETECTING AND/OR LOCATING FAULTY DATA WORDS IN A DATA STREAM T_N

IN THE CLAIMS

Please cancel claims 1-29 without prejudice.

Please add claims 30-63 as follows:

~~Patent Claims~~WHAT IS CLAIMED IS:

1-29. (Cancelled)

30. (New)An evaluation circuit comprising:

a first linear automation circuit;

a second linear automation circuit connected in parallel with the first linear automation circuit, each having a set of states, which have a common input line for receiving a data stream, wherein the first linear automaton circuit and the second linear automation circuit are configured such that a first signature and a second signature can be calculated;

a first logic combination gate and a second logic combination gate that compare the first signature and the second signature, respectively, with a predeterminable good signature and an output comparison value.

31. (New)The evaluation circuit as claimed in claim 30, comprising wherein the first logic combination gate and the second combination logic gate are exclusive-OR gates having first inputs, respectively, connected to the outputs of the associated first and second linear automaton circuit and to whose second inputs good signatures can be applied.

32. (New)The evaluation circuit as claimed in claim 30, comprising wherein arranged upstream of the first linear automaton circuit is a first coder, that codes the data word having the data word length of k bits into a coded data word $u^1(i)$, $u^1(i)$=Cod1 having the word width of K1 bits, for i=1, ..., n, and where Cod1 represents the coding function of the first coder.

33. (New)The evaluation circuit as claimed in claim 32, comprising wherein the following holds true for the coding function of the first coder (C1):

$$Cod1(y'(i)) = u^1(i) \oplus f_1(e(i)),$$

or

$$Cod1(y'(i)) = Cod1(y(i) \oplus e(i)) = Cod1(y(i) \oplus f_1(e(i))$$

where a function f_1 by $f_1(0) = 0$ exists for $y'(i) = y(i) \oplus e(i)$, and where a function f_1^{-1} where

$$f_1^{-1}(f_1(e)) = e$$

exists for all binary data words e having the word width k which may occur as errors of a data word, where e denotes a faulty data word of the data stream T_n.

34. (New)The evaluation circuit as claimed in one of claim 30, comprising wherein arranged upstream of the second linear automaton circuit is a second coder, which codes the data word y(i) having the data word length of k bits into a coded data word $u^2(i)$, $u^2(i)=Cod2(y(i))$ having the word width of K2 bits, for i=1, ..., n, and where Cod2 represents the coding function of the second coder (C2).

35. (New)An evaluation circuit for detecting and/or locating faulty data words in a data stream T_n comprising:

a first linear automaton circuit and a second linear automaton circuit connected in parallel, each having a set of states, wherein the first linear automaton circuit and the second linear automaton circuit have a common input line for receiving a data stream T_n comprising n successive data words y(1), ..., y(n) each having a width of k bits,

wherein the first linear automaton circuit can be described by the following equation

$$z(t+1) = Az(t) \oplus y(t)$$

wherein second linear automaton circuit can be described by the following equation

$$z(t+1) = Bz(t) \oplus y(t)$$

where A and B represent the state matrices of the linear automaton circuits, where the state matrices A and B can be inverted, and where the dimension L of the state vectors is ≥k,

the first linear automaton circuit and the second linear automaton circuit are designed such that a first signature and a second signature, respectively, can be calculated,

L first logic combination gates arranged downstream of the first linear automaton circuit and also L second logic combination gates arranged downstream of the second linear automaton circuit,

the logic combination gates are designed such that the signature respectively calculated by the linear automaton circuit can be compared with a predeterminable good signature and a comparison value can be output.

36. (New)The evaluation circuit as claimed in claim 35, comprising wherein the logic combination gates are present as exclusive-OR gates whose first inputs are respectively connected to the outputs of the associated linear automaton circuit (L1, L2) and to whose second inputs good signatures can be applied.

37. (New)The evaluation circuit as claimed in claim 35, comprising wherein arranged upstream of the first linear automaton circuit is a first coder, that codes the data word y(i) having the data word length of k bits into a coded data word $u^1(i)$, $u^1(i)$=Cod1 having the word width of K1 bits, for i=1, ..., n, and where Cod1 represents the coding function of the first coder.

38. (New)The evaluation circuit as claimed in claim 37, comprising wherein the following holds true for the coding function of the first coder:

$$\mathrm{Cod1}(y'(i)) = u^1(i) \oplus f_1(e(i)),$$

or

$$\mathrm{Cod1}(y'(i)) = \mathrm{Cod1}(y(i) \oplus e(i)) = \mathrm{Cod1}(y(i) \oplus f_1(e(i))$$

where a function f_1 by $f_1(0) = 0$ exists for $y'(i) = y(i) \oplus e(i)$, and where a function f_1^{-1} where

$$f_1^{-1}(f_1(e)) = e$$

exists for all binary data words e having the word width k which may occur as errors of a data word, where e denotes a faulty data word of the data stream T_n.

39. (New)The evaluation circuit as claimed in one of claim 35, comprising wherein arranged upstream of the second linear automaton circuit is a second coder, which codes the data word y(i) having the data word length of k bits into a coded data word $u^2(i)$, $u^2(i)=Cod2(y(i))$ having the word width of K2 bits, for i=1, ..., n, and where Cod2 represents the coding function of the second coder.

40. (New)The evaluation circuit as claimed in claim 39, comprising wherein the following holds true for the coding function of the second coder:

$$Cod2(y'(i)) = u^2(i) \oplus f_2(e(i)),$$

or

$$\begin{aligned} Cod2(y'(i)) &= Cod2(y(i) \oplus e(i)) \\ &= Cod2(y(i)) \oplus f_2(e(i)) \end{aligned}$$

where a function f_2^{-1} where

$$f_2^{-1}(f_2(e)) = e$$

exists for all binary data words e having the word width k which may occur as errors of a data word, where e denotes a faulty data word of the data stream T_n.

41. (New)The evaluation circuit as claimed in one of claim 37, comprising wherein that the word width K1 of the data words $u^1(i)$ coded by the first coder is equal to the word width K2 of the data words $u^2(i)$ coded by the second coder.

42. (New)The evaluation circuit as claimed in one of claim 37, comprising wherein the first coder matches the second coder with regard to its construction and its function.

43. (New)The evaluation circuit as claimed in one of claim 37, comprising wherein the word width K1 of the data words $u^1(i)$ coded by the first coder and the word width K2 of the data words $u^2(i)$ coded by the second coder are in each case equal to the word width k of the data words y(1), ..., y(n) of the data stream T_n.

44. (New)The evaluation circuit as claimed in one of claim 37, comprising wherein the coding functions Cod1 and Cod2 of the first coder and of the second coder are designed as follows:

$$\mathrm{Cod1}(y_1(i), y_2(i), \ldots, y_k(i))$$
$$= \mathrm{P1}(y_1(i), y_2(i), \ldots, y_k(i), 0, \ldots, 0)$$

$$\mathrm{Cod2}(y_1(i), y_2(i), \ldots, y_k(i))$$
$$= \mathrm{P2}(y_1(i), y_2(i), \ldots, y_k(i), 0, \ldots, 0)$$

for i, 1, ..., n

where the number of zeros situated at the end of $\mathrm{P1}(y_1(i), y_2(i), \ldots, y_k(i), 0, \ldots, 0)$ is equal to (K1-k), where the number at the end of $\mathrm{P2}(y_1(i), y_2(i), \ldots, y_k(i), 0, \ldots, 0)$ is equal to (K2-k), and where P1 represents an arbitrary permutation of the K1 components of $(y_1(i), y_2(i), \ldots, y_k(i), 0, \ldots, 0)$ and P2 represents an arbitrary permutation of the K2 components of $(y_1(i), y_2(i), \ldots, y_k(i), 0, \ldots, 0)$.

45. (New)The evaluation circuit as claimed in claim 37, comprising wherein the coding functions Cod1 and Cod2 of the first coder and of the second coderare designed as follows:

$$\mathrm{Cod1}(y_1(i), y_2(i), \ldots, y_k(i))$$
$$= \mathrm{P1}(y_1(i), y_2(i), \ldots, y_k(i), b_1^1 \ldots, b_{K1\ k}^1)$$

$$\mathrm{Cod2}(y_1(i), y_2(i), \ldots, y_k(i))$$
$$= \mathrm{P2}(y_1(i), y_2(i), \ldots, y_k(i), b_1^2 \ldots, b_{K2\ k}^2)$$

where $b_1^1, \ldots, b_{K1-k}^1, b_1^2, \ldots, b_{K2-k}^2 \in \{0.1\}$, and where P1 and P2 represent arbitrary permutations.

46. (New)The evaluation circuit as claimed in one of claim 37, comprising wherein the coding function Cod1 of the first coder is designed such that it realizes a linear block code, f_1=Cod1.

47. (New)The evaluation circuit as claimed in one of claim 37, comprising wherein the coding function Cod2 of the second coder is designed such that it realizes a linear block code, f_2=Cod2.

48. (New)The evaluation circuit as claimed in one of claim 35, comprising wherein the state matrix A of the first linear automaton circuit and the state matrix B of the second linear automaton circuit are related to one another as follows:

$$B = A^n$$

where $n \neq 1$.

49. (New)The evaluation circuit as claimed in claim 35, comprising wherein the state matrix B of the second linear automaton circuit is equal to the inverted state matrix A^{-1} of the first linear automaton circuit.

50. (New)The evaluation circuit as claimed in claim 35, comprising wherein the first linear automaton circuit is designed as a linear feedback shift register and the second linear automaton circuit is designed as an inverse linear feedback shift register, both linear automaton circuits having a parallel input.

51. (New)The evaluation circuit as claimed in claim 35, comprising wherein

the first linear automaton circuit is designed as a linear feedback, K1-dimensional multi-input shift register and/or the second linear automaton circuit is designed as a linear feedback, K2-dimensional multi-input shift register.

52. (New)The evaluation circuit as claimed in claim 51, comprising wherein the multi-input shift register/registers has/have a primitive feedback polynomial of maximum length.

53. (New)A method for detecting and/or locating faulty data words in a data stream T_n, the method having the following method steps of:

inputting data words y(1), ..., y(i-1), y'(i), y(i+1), ..., y(n) of a data stream T_n into a first coder,

coding the data words y(1), ..., y(n) into coded data words $u^1(1)$, ..., $u^1(n)$ having the word width K1 where K1≥k by means of the coding function Cod1 of the first coder,

inputting the coded data words $u^1(1)$, ..., $u^1(i-1)$, $u^{1}{'}(i)$ or $u^1(i)$, $u^1(i)$, ..., $u^1(n)$ into the inputs of a first linear automaton circuit, which is described by the automaton equation;

$z^1(t+1)=A\cdot z^1(t)+u^1(t)$

where z^1 represents a K1-dimensional state vector and A represents a K1×K1 state matrix, and where the state matrix A can be inverted,

processing the coded data words $u^1(1)$, ..., $u^1(i-1)$, $u^{1}{'}(i)$ or $u^1(i)$, $u^1(i)$, ..., $u^1(n)$ by means of the first linear automaton circuit, the first linear automaton circuit,

undergoing transition to the state $z^1(n+1)=S_1$(L1, y(1), ..., y(i-1), y(i), y(i+1), ..., y(n)) if no error can be detected in the case of the coded data words $u^1(1)$, ..., $u^1(i-1)$, $u^1(i)$, $u^1(i+1)$, ..., $u^1(n)$,

undergoing transition to the state $z^{1}{'}(n+1)=S_1$(L1, y(1), ..., y(i-1), y'(i), y(i+1), ..., y(n)) if an error is present at least in the case of the i-th position of the coded data words $u^1(1)$, ..., $u^1(i-1)$, $u^{1}{'}(i)$, ..., $u^1(n)$,

the signature of an error-free data stream T_n being designated by S(L1, y(1), ..., y(i-1), y(i), y(i+1), ..., y(n)) and the signature of a faulty data stream T_n being designated by S(L1, y(1), ..., y(i-1), y'(i), y(i+1), ..., y(n)),

checking the determined signature of the data stream T_n and continuing with method step a) for further data streams T_n if the determined signature of the data stream T_n is the signature of an error-free data stream T_n,

inputting the data words y(1), ..., y(i-1), y'(i), ..., y(n) of the data stream T_n in a second coder,

coding the data words y(1), ..., y(i-1), y'(i), y(i+1), ..., y(n) to coded data words $u^2(1)$, ..., $u^2(i-1)$, u^{2}'(i) or $u^2(i)$, $u^2(i)$, ..., $u^2(n)$ having the word width K2 where K2≥k by means of the coding function Cod2 of the second coder,

inputting the coded data words $u^2(1)$, ..., $u^2(i-1)$, u^{2}'(i) or $u^2(i)$, $u^2(i)$, ..., $u^2(n)$ into the inputs of a second linear automaton circuit, which is described by the automaton equation

$$z^2(t+1) = B \cdot z^2(t) \oplus u^2(t)$$

where z^2 represents a K2-dimensional state vector and B represents a K2xK2 state matrix where $B \neq A$, and where the state matrix B can be inverted,

processing the coded data words $u^2(1)$, ..., $u^2(i-1)$, u^{2}'(i) or $u^2(i)$, $u^2(i)$, ..., $u^2(n)$ by means of the second linear automaton circuit, the second linear automaton circuit,

undergoing transition to the state $z^2(n+1)=S_2$(L2, y(1), ..., y(i-1), y(i), y(i+1), ..., y(n)) if no error can be detected in the case of the data words $u^2(1)$, ..., $u^2(i-1)$, $u^2(i)$, $u^2(i)$, ..., $u^2(n)$,

undergoing transition to the state z^{2}'(n+1)=S_2(L2, y(1), ..., y(i-1), y(i), y'(i), y(i+1), ..., y(n)) if an error is present at least in the case of the i-th position of the coded data words $u^2(1)$, ..., $u^2(i-1)$, u^{2}'(i), $u^2(i)$, ..., $u^2(n)$,

the signature of an error-free data stream T_n being designated by S(L2, y(1), ..., y(i-1), y(i), y(i+1), ..., y(n)) and the signature of a faulty data stream T_n being designated by S(L2, y(1), ..., y(i-1), y'(i), ..., y(n)),

determining the signature differences $\Delta S1$ and $\Delta S2$ by means of exclusive-OR logic combinations of the signatures S1 and S2 determined in method step d) and i), respectively, with ascertained good signatures, in each case according to the following specifications:

$$\Delta S1 = S(L1, y(1), ..., y(i-1), y(i), y(i+1), ..., y(n))$$
$$\oplus\ S(L1, y(1), ..., y(i-1), y'(i), y(i+1)..., y(n))$$

$$\Delta S2 = S(L2, y(1), ..., y(i-1), y(i), y(i+1), ..., y(n))$$
$$\oplus\ S(L2, y(1), ..., y(i-1), y'(i), y(i+1), ..., y(n))$$

determining a unique solution for the position i of the faulty bit in the faulty data word by solving the equation

$$f_1^{-1}(A^{i-n}\Delta S1) = f_2^{-1}(B^{i-n}\Delta S2)$$

and if no unique solution results for $1 \leq i \leq n$, outputting a notification by means of an output medium that two or more errors are present in the data stream T_n under consideration,

determining a unique solution for the counter e(i) of the faulty data word y'(i) in the data stream T_n by solving the equation

$$e(i) = f_1^{-1}(A^{i-n} \cdot \Delta S1)$$

outputting the position i of the faulty bit in the faulty data word and also the error e(i) of the faulty data word y'(i) in the data stream T_n by means of an output medium.

54. (New)The method as claimed in claim 53, comprising wherein the method is carried out by means of an evaluation circuit as claimed in one of claim 35.

55. (New)The evaluation circuit as claimed in one of claim 35, comprising wherein the evaluation circuit is monolithically integrated on an integrated circuit.

56. (New)A loadboard for receiving at least one needle card for testing integrated circuits and/or having at least one test socket for testing integrated circuits and/or for connecting a

handler to a tester of integrated circuits, the loadboard having an evaluation circuit as claimed in one of claim 35.

57. (New)A needle card for testing integrated circuits, in which an evaluation circuit as claimed in one of claim 35 is integrated.

58. (New)A tester for testing integrated circuits having the following features:

the tester is provided with a plurality of instruments for generating signals or data streams and with a plurality of measuring sensors, in particular for currents and voltages,

the tester has a loadboard which is provided for receiving at least one needle card for testing integrated circuits and/or for connecting a handler to a tester of integrated circuits and/or which is equipped with at least one test socket for testing integrated circuits, and

the tester has an evaluation circuit as claimed in one of claim 35.

59. (New)A computer program for executing a method for detecting and/or locating faulty data words in a data stream T_n, which is designed for executing a portion of the method of claim 53.

60. (New)The computer program as claimed in claim 59, which is contained on a storage medium, in particular in a computer memory or in a random access memory.

61. (New)The computer program as claimed in claim 59, which is transmitted on an electrical carrier signal.

62. (New)A data carrier having a computer program as claimed in claim 59.

63. (New)A method in which a computer program as claimed in claim 57 is downloaded from an electronic data network onto a computer connected to the data network.